

REMARKS

Applicants acknowledge with thanks the interview granted by the Examiner on April 29, 2002.

Claims 1-10 and 29-31 stand rejected under 35 U.S.C. § 103(a) "as being unpatentable over Applicant's Specification in view of Matsuura et al." (U.S. Patent No. 5,132,774).

Reconsideration and allowance of claims 1, 3-10 and 29-31, and consideration and allowance of claim 32, are respectfully requested for the reasons set forth below.

During the telephone interview on April 29, 2002, Applicants' representative discussed claim 2 with the Examiner. Claim 2 has been cancelled, and claim 1 has been amended to include the features of claim 2. Before being cancelled by the present amendment, claim 2 of the present application recited that the dielectric film in the capacitor "is formed from either a dielectric material having a high dielectric constant or a ferroelectric material." As discussed in the interview, this feature is recited in Applicants' Specification not as prior art, but to demonstrate the problems that Applicants discovered with respect to second interlayer insulating films having compressive stress in capacitor semiconductor devices. Further, Matsuura does not disclose or suggest this feature. Therefore, Applicants' representative argued against the rejection of claim 2 under 35 U.S.C. § 103(a) "as being unpatentable over Applicant's Specification in view of Matsuura et al." During the interview, the Examiner gave merit to this argument. The Examiner indicated that an additional search would be conducted to look for a single piece of prior art that discloses a capacitor having the characteristics recited in claim 2, where the capacitor is part of a semiconductor device including a second interlayer insulating film having tensile stress. If this additional search does not reveal such a reference, the Examiner indicated that the rejection of claim 1 (including the features of cancelled claim 2) would be withdrawn. If such a piece of prior art is located by the Examiner, Applicants respectfully remind the Examiner that the rejection should not be made final, because there has been no amendment of claim 2 necessitating the additional search.

Claims 3-10 and 29 are dependent on claim 1. As such, if the rejection of claim 1 is withdrawn, claims 3-10 and 29 should be allowed.

Claims 30 and 31 have been amended to be in independent form, and as such, claims 30 and 31 include all of the features of the previous version of claim 1. This version of claim 1 was the version of claim 1 upon which claims 30 and 31 depended at the time of the telephone interview. Claim 30 includes the feature of the dielectric film having "a remnant polarization of approximately $10 \mu\text{C}/\text{cm}^2$." Claim 31 includes the feature of the dielectric film having "a remnant polarization of at least $10 \mu\text{C}/\text{cm}^2$." Neither of these features is disclosed in the Matsuura reference. Therefore, during the interview, Applicants' representative argued that the rejection of claims 30 and 31 under 35 U.S.C. § 103(a) "as being unpatentable over Applicant's Specification in view of Matsuura et al." was improper. The Examiner gave merit to this argument. The Examiner indicated that an additional search would be conducted to look for a single reference disclosing a semiconductor device including a second interlayer insulating film having tensile stress, the semiconductor device including a capacitor having the characteristics set out in claims 30 and 31. Applicants remind the Examiner that if such a reference is located, then the rejection should not be made final, because there has been no amendment of claims 30 and 31 necessitating a new search. During the interview, the Examiner indicated that if such a reference was not located, the rejection of claims 30 and 31 would be withdrawn.

During the interview, the Examiner also stated that if the second interlayer insulating film was more specifically defined in claim 1, then amended claim 1 may overcome the present rejection. Claim 8, which depends from claim 1, includes the feature of the second interlayer insulating film having "a tensile stress of $1 \times 10^7 \text{ dyn}/\text{cm}^2$ to $3 \times 10^9 \text{ dyn}/\text{cm}^2$ inclusive." In the Office Action dated April 9, 2002, Official Notice was taken with respect to this limitation. Specifically, the Office Action indicated that one of ordinary skill in the art would modify the second interlayer insulating film of Matsuura to have a tensile stress of about $3 \times 10^9 \text{ dyn}/\text{cm}^2$. In taking this Official Notice, the Examiner cited Table 2 of Wolf et al. (see "Silicon Processing for the VLSI Era Volume 1: Process Technology", Lattice Press, 1986, pp. 182-194). Therefore, the rejection of claim 8 is a combination of Applicants' Specification, Matsuura, and Official Notice taken in view of Wolf. Applicants respectfully request reconsideration of claim 8

because of an improper combination of references. Specifically, there is no motivation to combine the tensile stress value included in Table 2 of Wolf with Applicants' Specification or Matsuura. This is especially true in light of the fact that Applicants discovered the benefits of providing a semiconductor device including a capacitor, the device also including a second interlayer insulating film with a tensile stress in the range recited in claim 8.

Applicants' invention, as recited by newly added claim 32 includes a feature which is neither disclosed nor suggested by the art of record, namely:

the first interlayer insulating film having a tensile stress.

This means that the semiconductor device recited in claim 32 includes a first interlayer insulating film, as well as a second interlayer insulating film, both of the films having tensile stress. Further, the first interlayer insulating film recited in claim 32 directly covers the capacitor. Therefore, there is no additional film between the capacitor and the first interlayer insulating film.

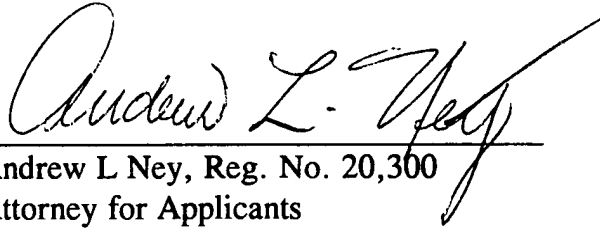
Neither Matsuura nor Wolf recite a semiconductor device that includes a first interlayer insulating film directly covering a capacitor that has tensile stress.

It is because Applicants include the feature of the first interlayer insulating film that has a tensile stress that the following advantages are achieved. The first interlayer insulating film, having tensile stress, provides a sufficient flat top surface with substantially no step. Therefore, a thin first interlayer insulating film is provided, and stress on the capacitor resulting from the prior art first interlayer insulating films is alleviated. As such, a capacitor with superior electrical characteristics is provided.

Accordingly, for the reasons set forth above, claim 32 is patentable over the art of record.

In view of the foregoing amendments and remarks, this application is in condition for allowance, unless the further searches by the Examiner turn up relevant prior art.

Respectfully Submitted,


Andrew L Ney, Reg. No. 20,300
Attorney for Applicants

ALN/ap

Enclosures:

Version with markings to show changes made

Dated: July 9, 2002

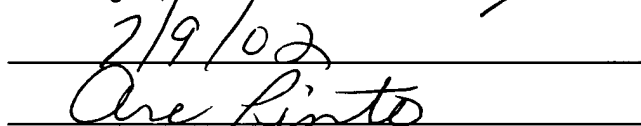
P.O. Box 980

Valley Forge, PA 19482-0980

(610) 407-0700

The Assistant Commissioner for Patents
is hereby authorized to charge payment
to Deposit Account No. 18-0350 of any
fees associated with this communication.

I hereby certify that this correspondence is being
deposited with the United States Postal Service with
sufficient postage as first class mail in an envelope
addressed to: Assistant Commissioner for Patents,
Washington, D.C. 20231 on:



Are Linto

VERSION WITH MARKINGS TO SHOW CHANGES MADECLAIMS:

- 1 1. (As Amended) A semiconductor device, comprising:
- 2 a capacitor provided on a supporting substrate having an integrated
- 3 circuit thereon and including a lower electrode, a dielectric film, and an upper
- 4 electrode, said dielectric film being formed from either a dielectric material having
- 5 a high dielectric constant or a ferroelectric material;
- 6 a first interlayer insulating film provided so as to directly cover the
- 7 capacitor;
- 8 a first interconnect selectively provided on the first interlayer
- 9 insulating film and electrically connected to the integrated circuit and the capacitor
- 10 through a first contact hole formed in the first interlayer insulating film;
- 11 a second interlayer insulating film having a tensile stress provided so
- 12 as to directly cover the first interconnect and the first interlayer insulating film;
- 13 a second interconnect selectively provided on the second interlayer
- 14 insulating film and electrically connected to the first interconnect through a second
- 15 contact hole formed in the second interlayer insulating film; and
- 16 a passivation layer provided so as to cover the second interconnect.

- 1 30. (Amended) A semiconductor device, comprising:
- 2 a capacitor provided on a supporting substrate having an integrated
- 3 circuit thereon and including a lower electrode, a dielectric film, and an upper
- 4 electrode, said dielectric film including a remnant polarization of approximately 10
- 5 $\mu\text{C}/\text{cm}^2$;
- 6 a first interlayer insulating film provided so as to directly cover the
- 7 capacitor;

8 a first interconnect selectively provided on the first interlayer
9 insulating film and electrically connected to the integrated circuit and the capacitor
10 through a first contact hole formed in the first interlayer insulating film;

11 a second interlayer insulating film having a tensile stress provided so
12 as to directly cover the first interconnect and the first interlayer insulating film;

13 a second interconnect selectively provided on the second interlayer
14 insulating film and electrically connected to the first interconnect through a second
15 contact hole formed in the second interlayer insulating film; and

16 a passivation layer provided so as to cover the second interconnect.

17 [The semiconductor device of claim 1 wherein the dielectric film
18 includes a remnant polarization of approximately $10 \mu\text{C}/\text{cm}^2$.]

1 31. (Amended) A semiconductor device, comprising:

2 a capacitor provided on a supporting substrate having an integrated
3 circuit thereon and including a lower electrode, a dielectric film, and an upper
4 electrode, said dielectric film including a remnant polarization of at least 10
5 $\mu\text{C}/\text{cm}^2$;

6 a first interlayer insulating film provided so as to directly cover the
7 capacitor;

8 a first interconnect selectively provided on the first interlayer
9 insulating film and electrically connected to the integrated circuit and the capacitor
10 through a first contact hole formed in the first interlayer insulating film;

11 a second interlayer insulating film having a tensile stress provided so
12 as to directly cover the first interconnect and the first interlayer insulating film;

13 a second interconnect selectively provided on the second interlayer
14 insulating film and electrically connected to the first interconnect through a second
15 contact hole formed in the second interlayer insulating film; and

16 a passivation layer provided so as to cover the second interconnect.

- 17 [The semiconductor device of claim 1 wherein the dielectric film
18 includes a remnant polarization of at least $10 \mu\text{C}/\text{cm}^2$.]

Claim 2 has been cancelled.

Claim 32 has been newly added.